Sea-of-Leads MEMS I/O Interconnects for Low-k IC Packaging

Bing Dang, *Student Member, IEEE*, Muhannad S. Bakir, *Member, IEEE*, Chirag S. Patel, Hiren D. Thacker, *Member, IEEE*, and James D. Meindl, *Life Fellow, IEEE*

***Abstract*—Technology feasibility of MEMS-type chip I/O interconnects (namely Sea-of-Leads or SoL) is demonstrated. Acting like a spring, a MEMS lead can provide high mechanical compliance to compensate for mismatch of coefficient of thermal expansion (CTE) between a Si chip and a composite substrate. The compliant interconnects can provide low-stress connection between a chip and a PWB substrate, and, therefore, are promising to enable wafer-level packaging of IC chips with mechanically weak low-k interlayer dielectrics (ILD). The compliant interconnection also eliminates the need for an expensive underfilling process, which is one of the key challenges for scaling of conventional controlled collapse chip connection (C4) solder bumps in organic flip-chip packages. For the first time, SoL MEMS interconnects were investigated through the whole procedure of process integration, assembly, as well as reliability assessment. Without underfill, the SoL MEMS interconnects survived more than 500 thermal cycles indicating a promising improvement over a regular C4 solder joint. Failure analysis suggests that the MEMS leads do not fracture while failure occurs close to solder-Cu pad interface due to a nonreliable joining. Full reliability potential of the SoL MEMS interconnects may be demonstrated upon optimization of PWB metallurgy, soldermask design and lead compliance. [1558]**

***Index Terms*—Low-k interlayer dielectrics, microelectromechanical systems (MEMS) I/O interconnects, solder joints, underfill.**

I. Introduction

IC-to-Substrate interconnect pitch is being continuously scaled down to provide very high area array I/O density according to the International Technology Roadmap for Semiconductors [1]. Thus, the dimension of the C4 solder joints in flip-chip packages must be reduced accordingly. Because of the CTE mismatch between Si and organic PWB substrate, the shear strain on a C4 solder joint will increase significantly for the reduced stand-off height. Although underfill is widely used to enhance the reliability of flip-chip packages, the underfilling process will be difficult for such a small gap between a chip and a substrate. Application of underfill also raises numerous problems including poor reworkability, time-consuming processes, and electrical performance degradation. In addition, as low-k ILD materials are being widely pursued to improve electrical performance of microprocessors, thermal–mechanical stress has reportedly led to delamination of bonding pads due to the weak mechanical strength and poor adhesion strength of the porous low-k dielectric materials [2]–[4]. To reduce the cost and complexity of high I/O count area-array packages, wafer-level packaging with novel I/O interconnects are necessary.

Compliant interconnects are an attractive solution for these problems because they can compensate for the CTE mismatch between a Si chip and an organic PWB substrate. Compliant interconnects can be fabricated in wafer-level at low cost and can potentially eliminate the need for underfill after assembly, and, therefore, can enable wafer-level chip-scale packages. In recent years, several compliant interconnect technologies [5]–[10] have been studied. FormFactor's WOW technology utilizes a wire-bonder [5] to fabricate microsprings for wafer level packages, however, the serial operation of wire-bonding is time-consuming for high I/O count applications. Tessera's WOW technology uses batch fabrication but involves transient-liquid-phase Cu bonding and wafer-level injection encapsulation processes [6]. These operations are not commonly available in the standard back-end-of-line (BEOL) facilities. The helix-type interconnects are monolithically fabricated but require multiple electroplating steps and a long RIE etch-back to remove the thick photoresist [7], [8].

Compared to other compliant interconnect technologies, Sea-of-Leads (SoL) technology simply extends BEOL process to provide chip interconnection with high I/O density at the wafer level [9]. SoL fabrication only requires the standard wafer processing techniques and can be easily incorporated in conventional wafer-bumping and packaging processes. The I/O pitch can be easily scaled down for high I/O density. Particularly, a "slippery type" SoL is promising, as it offers the maximum effective in-plane compliance once adhesion to the polymer film is eliminated. Such a lead structure is essentially a MEMS interconnect, which has spring-like behavior for high thermal-mechanical reliability. However, several issues must be addressed for this MEMS-type SoL. First, a manufacturable release approach is needed and a certain sacrificial layer is necessary. Second, a suitable solder bumping scheme must be developed for joining with the package substrate, which requires a solder dam/barrier to effectively confine the solder bump to avoid wicking of the metal leads [11]. Meanwhile, the solder barrier/dam should not restrict the compliance of a lead.

Manuscript received March 25, 2005; revised July 12, 2005. This work was carried out as part of the Interconnect Focus Center Research Program at the Georgia Institute of Technology. This work was supported in part by the Microelectronics Advanced Research Corporation (MARCO), its participating companies, and DARPA under Contract 2003-IT-674. Subject Editor N. C. Tien.

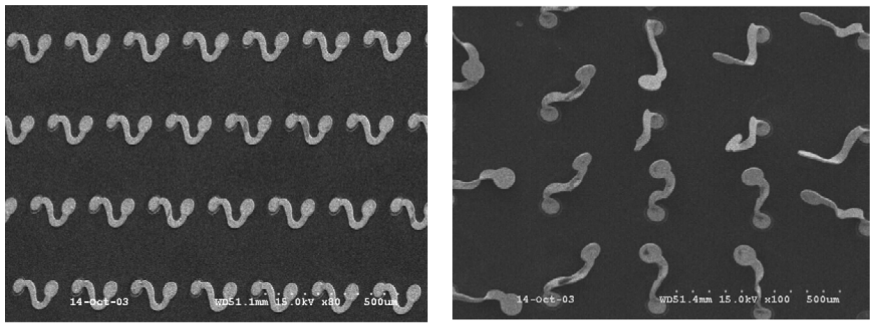
B. Dang, M. S. Bakir, H. D. Thacker, and J. D. Meindl are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Microelectronics Research Center, Atlanta, GA 30332 USA (e-mail: dangbing@ece.gatech.edu).

C. S. Patel is with the IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA.

Digital Object Identifier 10.1109/JMEMS.2006.876792

TABLE I
SUMMARY OF THE SACRIFICIAL MATERIALS FOR RELEASING OF MEMS LEADS AS I/O INTERCONNECTS

Sacrificial Materials	Photoresist	Al thin film	Decomposable Polymer
Deposition method	Spin coating	DC Sputtering, Evaporation etc.	Spin-coating
Removal method	Dissolving with solvents	Selective etching	Heating at ~170ºC



(a) metal leads after removal of sacrificial layer (b) an area after peeling by adhesive tape

Fig. 1. SEM photographs of electroplated leads after (a) release process and (b) the destructive peeling test to confirm that the leads are flexible but well anchored.

Finally, to evaluate the reliability of the SoL interconnects on the low-cost PWB substrate, handling and assembly challenges associated with their flexible nature should be overcome.

In this paper, fabrication processes of the SoL MEMS interconnects were developed to achieve high manufacturing yield and high reliability. Section II presents the integration process with a BEOL wafer, which requires three additional mask steps compared to the conventional C4 bumping process. In Section III, benefits of MEMS interconnects on low-k interconnects are discussed with micromechanical modeling. In Section IV, handling and assembly issues associated with the compliant interconnects are discussed and the bonding experiments of SoL test chips onto organic PWB test vehicle are presented. Section V presents the preliminary reliability results of SoL wafer-level packages and the failure mechanism discussion. Section VI is the conclusion.

II. FABRICATION AND INTEGRATION OF SOL MEMS INTERCONNECTS

The "lift-off" release method with a sacrificial layer is commonly used to fabricate MEMS structures such as cantilevers and actuators [12], [13]. In this paper, a similar approach is adopted to release the metal leads to become compliant chip I/O interconnects. Three types of sacrificial materials were investigated as listed in Table I. They are a photoresist, Al thin-film, and thermally decomposable polymer film (polynorbornene). A photoresist was first selected because it can be easily removed. A 2-μm-thick Shipley 1827 photoresist can be simply patterned as a sacrificial layer but an extra hard bake step (15 min at 110 °C) must be performed to prevent its thermal deformation during the subsequent steps. The thin film Al does not have issue of thermal deformation and can be deposited by dc sputtering or evaporation. It can be selectively etched with diluted NaOH solution, which is fairly benign to the electroplated leads (Au or Cu). In addition, a low-temperature decomposable polymer, Unity 200 (Promerus LLC) was also experimented. The polypropylene carbonate-based sacrificial polymers can be spin-coated and photodefined. When heated to 170 °C for 30 mins, the polymer film can be decomposed.

Nevertheless, by means of the sacrificial layer, such a lift-off process can ensure low cost and high manufacturing yield. A destructive peeling test has been performed to confirm success of the process. Fig. 1(a) is the SEM photograph of metal leads after removal of the sacrificial layer. Fig. 1(b) shows the SEM image for the area tested with adhesive tape, which clearly indicates that the metal leads have been released and none of the leads were detached because the via end of the leads is well anchored.

Based on the above approach, the process integration of SoL for wafer-level packaging is illustrated in Fig. 2, which requires three additional mask steps compared with the standard C4 bumping process. As shown in Fig. 2(a), fabrication of SoL begins with a completed BEOL wafer with via through a final passivation (Si_3N_4 or polymer). A sacrificial layer is first deposited and patterned with the via mask [Fig. 2(b)]. A seed layer of Ti/Cu (30/200 nm) was then deposited [Fig. 2(c)]. Metal leads were plated in a photoresist mold defined by photolithography [Fig. 2(d)]. In this paper, Au leads were used for a better corrosion resistance and fatigue resistance. The seed layer also acts as a strong adhesion layer for the electroplated leads. A solder barrier/dam was fabricated with a photodefinable dielectric polymer (Avatrel 2000P, Promerus LLC) over a metal lead and patterned such that it does not restrict its displacement [Fig. 2(e)]. The polymer was cured at 160 °C $T_g > 250$ °C. After that, a thicker photoresist was used to define the bump area at the end of each lead. A 3-μm Ni layer was first electroplated as the under bump metallurgy (UBM) and followed by Sn60Pb40 solder bump plating [Fig. 2(f)]. Ni-UBM is selected because Ni-Sn intermetallics provide reliable joining interface [15], [16]. After the photoresist was stripped, the seed layer was etched away and the sacrificial layer was removed [Fig. 2(g)]. After reflow with flux, solder bumps with spherical shape were formed onto the MEMS leads [see Fig. 2(h)].

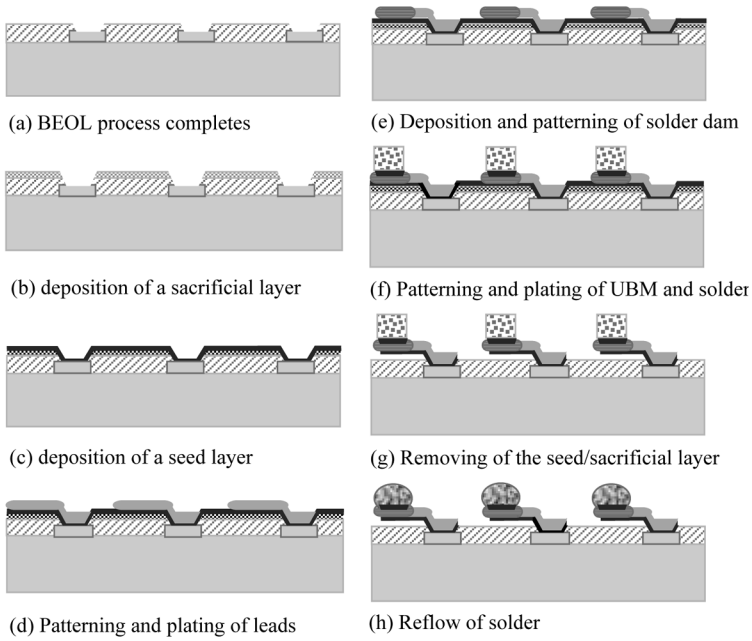
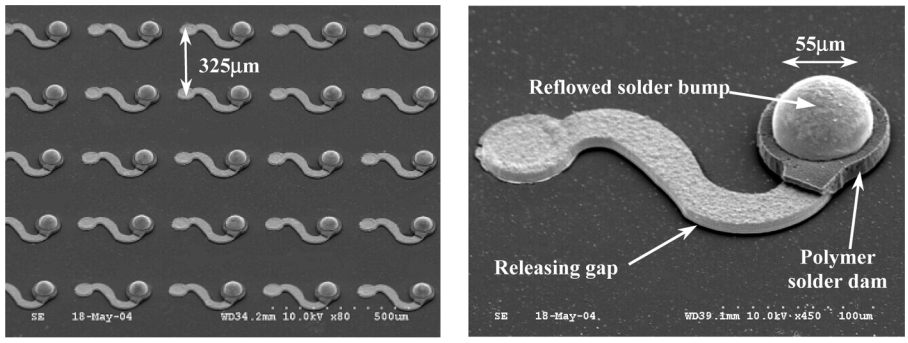


Fig. 2. Illustration of the integration of slippery SoL interconnects with a BEOL wafer.



(a) overview (b) perspective view

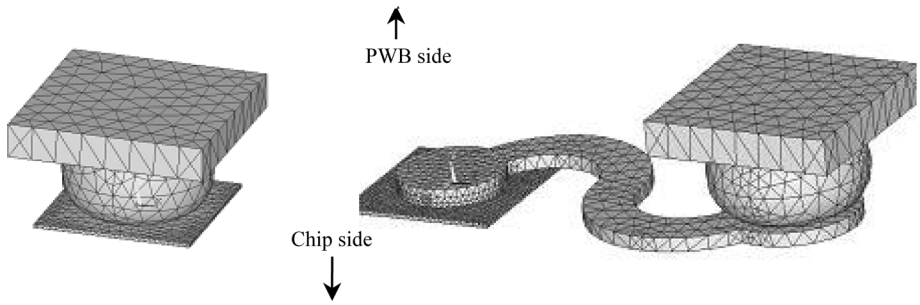
Fig. 3. SEM photographs of the completed SoL MEMS interconnects ($h_{\mathrm{gap}} \sim 2\ \mu\mathrm{m}$; $t_{\mathrm{lead}} \sim 7\ \mu\mathrm{m}$; $t_{\mathrm{UBM}} \sim 3.5\ \mu\mathrm{m}$; $h_{\mathrm{bump}} \sim 25\ \mu\mathrm{m}$; overall height $\sim 42.5\ \mu\mathrm{m}$).

Fig. 3 shows SEM images of the completed SoL interconnects on a test chip. A releasing gap left by the sacrificial layer is clearly visible below the Au lead. The solder dam surrounding a bump effectively protects a lead from being wicked by the solder during reflow. The total stand-off height of a completed interconnect is 42.5 $\mu\mathrm{m}$ approximately, which includes the gap between the lead and the chip passivation, the thickness of the lead, the thickness of the solder dam, the thickness of the Ni-UBM, and the thickness of the final solder bump height.

III. Mechanical Benefits of the SoL MEMS I/O Interconnects

Chip-packaging interaction becomes a critical reliability issue as the mechanically weak low-k ILD materials are used in the advanced ICs. Wang [3] and Mercado [4] have recently studied the impact of flip chip packaging on the Cu/low-k interconnect structure. They concluded that although underfill is beneficial to the reliability of chip-package interconnects (solder joints), it strongly couples a chip with the package substrate since underfill would restrict the free expansion of the substrate. The deformation leads to a large shear force on the chip surface [3], which ultimately induces crack and interfacial delamination of the Cu/low-k interconnects. The motivation of MEMS I/O interconnects is to mechanically decouple the chip pads from the deformation of the organic package substrate. Without use of underfill, the unique geometries of SoL interconnects accommodate the CTE mismatch between a Si chip and an organic package.

Finite-element analysis (FEA) models were built to compare a C4 solder joint with a SoL MEMS interconnect as a chip-package interconnect (Fig. 4). In the FEA models, the solder joints have a highly collapsed spherical shape because of the compression force used in the experiments during the flip-chip bonding. A solder joint is 40 $\mu\mathrm{m}$ in height and the contact area on a pad is 55 $\mu\mathrm{m}$ in diameter. The materials' models used to represent the behavior of the various components in the FEA models are listed in Table II. The time independent plastic behavior of both Cu and Au were represented utilizing a classical bilinear kinematic hardening rule, while 60Sn40Pb solder

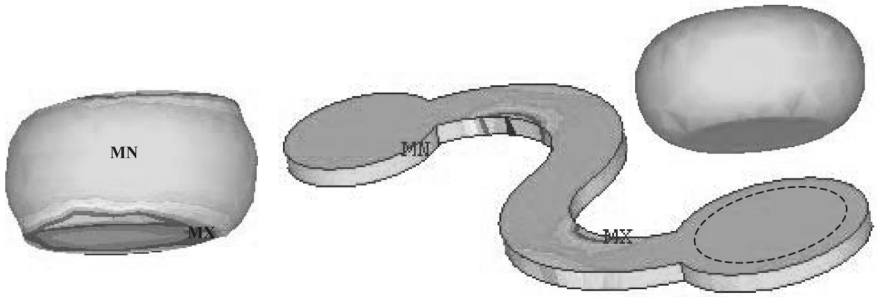


(a) C4 solder joint (b) SoL MEMS interconnect

Fig. 4. The meshed 3-D FEA models of a C4 solder joint and a SoL as the interconnect between chip-package bonding pads (chip pad: 80 μm $\times$ 80 μm $\times$ 2 μm; PWB pad: 100 μm $\times$ 100 μm $\times$ 9 μm; $h_{\mathrm{solder}} = 40\ \mu\mathrm{m}$; $D_{\mathrm{contact}} = 55\ \mu\mathrm{m}$).

TABLE II
MATERIALS PROPERTIES FOR FEA MODELS

Materials	Components	Material Model	Modulus (GPa)	Poisson's ratio
Cu	Chip pad, PWB pad, MEMS lead	Bilinear kinematic hardening rule	121	0.3
Au	MEMS lead	Bilinear kinematic hardening rule	64	0.42
60Sn40Pb	Solder joint	Multilinear kinematic hardening rule	30.685- (nonlinear)	0.4



(a) a C4 solder joint (b) a MEMS lead with a C4 solder joint

Fig. 5. Von-mises plastic strain distribution caused by an in-plane displacement between a chip pad and a PWB pad (a) with a C4 solder joint as the interconnect or (b) with a MEMS lead with a C4 solder joint as the interconnect.

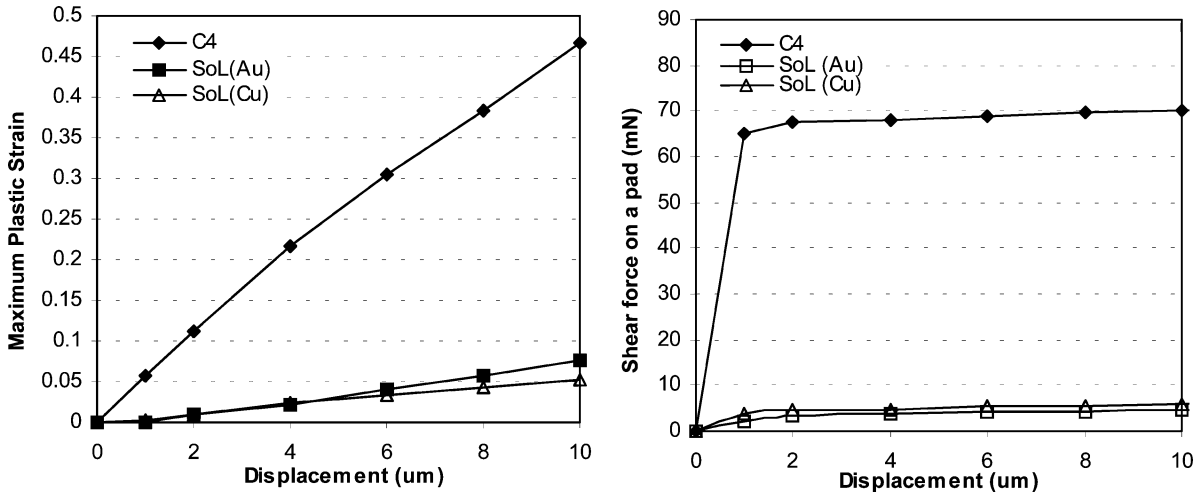
was represented utilizing a multilinear kinematic hardening rule. The creep behavior of the solder was not modeled.

Using ANSYS, the relative shear displacement between a chip pad and its counterpart pad on the package substrate was simulated for a single C4 solder joint and a SoL interconnect. During the simulation, the bonding pad at the chip side was constrained, while a displacement was applied on the PWB Cu pad. Due to the difference in geometry, mechanical structure, and material properties, the response from the displacement is significantly different for a C4 solder joint and a SoL MEMS interconnect. As shown in Fig. 5(a), with a C4 solder joint as the interconnect, both sides of the joint are strained and the maximum plastic strain is located at the solder-pad interface at the chip side. When a MEMS lead is used as the interconnect, the maximum plastic strain is located in the curved lead instead. No significant deformation occurs in the solder joint [Fig. 5(b)].

In Fig. 6(a), the maximum plastic strain is plotted as a function of the relative displacement for the two types of interconnects. The maximum plastic strain level induced in a MEMS interconnect is significantly smaller than that induced in a regular C4 solder joint. SoL MEMS interconnects are, therefore, promising to offer high reliability. In addition, the induced shear force is plotted as a function of the in-plane displacement as shown in Fig. 6(b). The shear force exerted by a C4 solder joint is more than 10 times higher than that from a MEMS lead. Since the force exerted on a chip pad will impact the reliability of the on-chip interlayer dielectrics (ILD), the advantage of compliant interconnects for the fragile low-k ILD is clearly illustrated. A Cu lead induces slightly higher force than an Au lead due to its larger modulus. The induced plastic strain will be further minimized and the effective compliance (displacement/force ratio) will be improved through optimization of the lead design through altering of geometry parameters such as radius and orientation of the various portions of a lead.

IV. HANDLING AND ASSEMBLY ISSUES OF SOL CHIP

Although the highly compliant interconnects are desirable in terms of reliability, a great challenge is to protect them from damage before assembly. For example, high-pressure DI water



(a) the maximum von-mises plastic strain (b) the induced shear force on a pad

Fig. 6. Mechanical response as a function of the relative displacement for a C4 solder joint or a SoL MEMS interconnect as the chip-package interconnect.

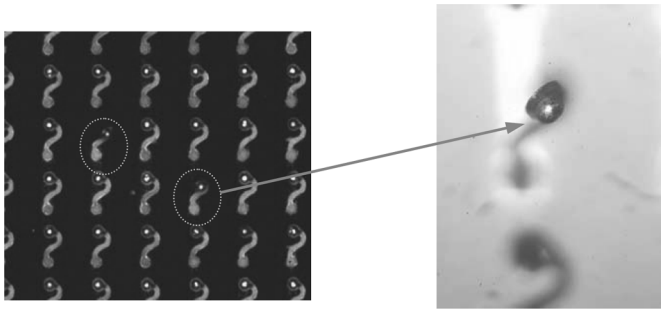


Fig. 7. Illustration of a handling issue during the dicing process with high pressure DI water.

during a dicing process can lift up or deform the compliant leads excessively in some areas if the leads are not protected (Fig. 7). An effective approach to avoid this problem is to encapsulate the leads with a dissolvable polymer film such as photoresist before wafer dicing. This approach is commonly used for the MEMS wafers when the surface is sensitive to the dicing dust or high-pressure water flow in the dicing process. The encapsulant can be removed by solvents during a post-dicing clean operation.

After the SoL chips are diced and cleaned, the next step is the assembly. In this study, a flip-chip bonder with high accuracy was used (RD Automation Inc, Model MA-10). The major challenges include lead wicking by solder under excessive compression and displacement of the "slippery" MEMS leads under compression. Therefore, bonding experiments with various profiles (temperature, force, and reflow time) were conducted to find an optimized process as shown in Fig. 8.

A transparent glass substrate was first used for the purpose of easy inspection. During bonding, a thin layer of flux was applied to promote soldering and a compression force ($\sim$250 g) was loaded on the backside of a SoL chip. The reflow temperature is 220 °C. Under profile A, a compression force is loaded first and the temperature is then raised; Under profile B, temperature is increased first and the compression force is applied after the temperature reaches the reflow temperature; under profile C, the compression force is maintained before and during the reflow process and the force is released after the chip is cooled down below the melting temperature of the 60Sn40Pb solder ($\sim$183 °C). Optical inspection and electrical continuity test were performed to verify the bonding yield. The best bonding yield was obtained under profile C. To perform the thermal mechanical reliability test, a test vehicle was built with a low-cost FR-4 laminate and eight SoL chips have been bonded on the test vehicle as shown in Fig. 9. X-ray microscopy confirms the accurate alignment of the bonded leads on the PWB Cu pads.

V. Thermal Mechanical Reliability Test and Failure Analysis

The test chips used 1 cm × 1 cm in size and each chip contains 31 parallel daisy chains at pitch of 325 μm. Each daisy chain consists of 30 leads and solder joints cascaded between the chip and the board. Fifty-four functional chains were tested in total and the average measured chain resistance of the as-bonded samples is 2.52 Ω, which agrees with the calculated value. The SoL test vehicles were then subjected to thermal cycling between 0 °C–100 °C for the accelerated temperature cycling test based on JEDEC Standard (Condition J of JESD 22-A104-B). The dwell time at the upper and lower zones is 15 min, respectively, with two cycles/h.

Fig. 10(a) shows the cross-sectional view of a typical solder joint connecting a metal lead and a Cu pad on the test board. Uniform interface can be observed at the boundary between the solder and the Ni-UBM. Meanwhile, an obvious intermetallic compound (IMC) layer is observed at the solder-Cu pad boundary. Fig. 10(b) plots the accumulative failure rate versus number of thermal cycles. After 100 cycles, 13% test chains failed with open circuit tested. All the test chains failed after 523 thermal cycles.

To understand the main failure mechanism of the SoL compliant interconnects, various failure observations were performed. Several failed chips were first removed at 220 °C as illustrated in Fig. 11. Since there was no underfill, the chip can be easily removed by a piece of polyimide tape once heated up.

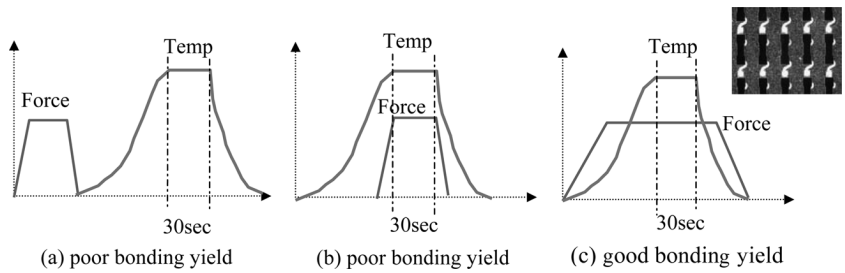


Fig. 8. Various temperature-force profiles of in bonding experiments (profile A and B give poor bonding yield while a good bonding yield was obtained under profile C).

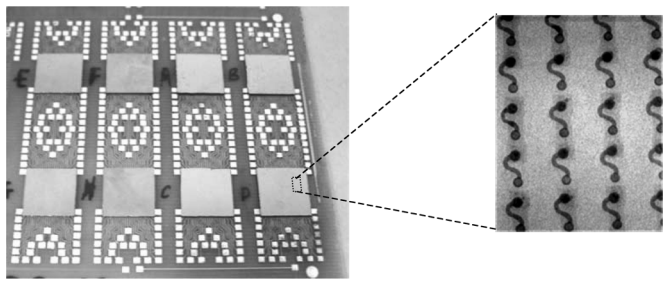


Fig. 9. Overview of SoL chips bonded on the FR-4 test vehicle and X-ray microscopy that shows successful joining of compliant interconnects.

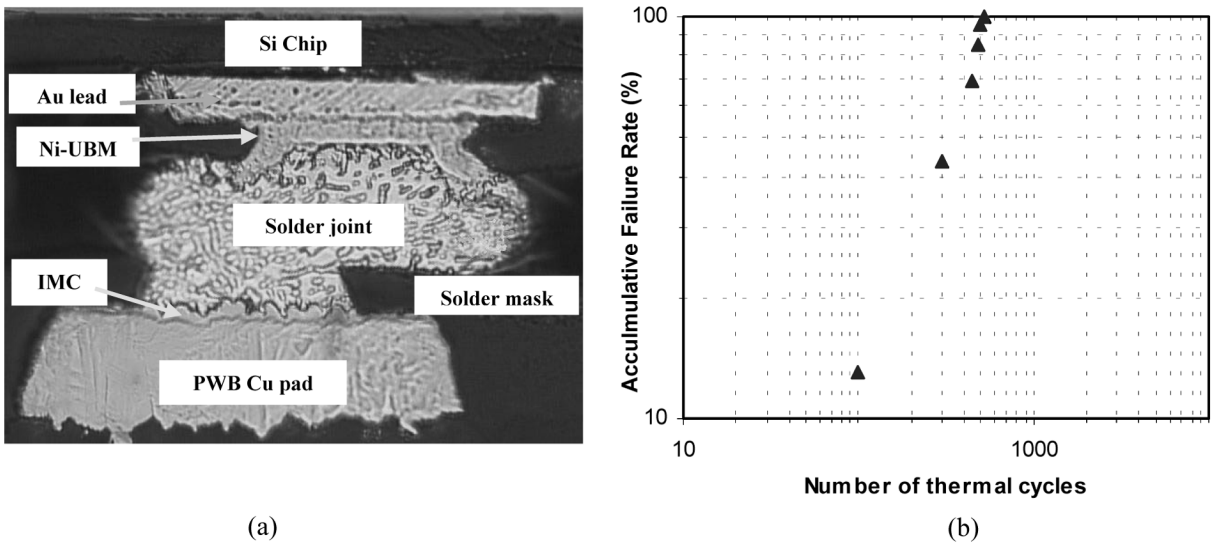


Fig. 10. (a) Cross-sectional view of a solder joint connecting a MEMS lead with a Cu pad on the PWB substrate (b) resistance change on a daisy chain during the thermal cycling test.

In this way, the solder was melted first and the interconnects were preserved for inspection. As shown in the Fig. 11, none of the MEMS leads were broken during the thermal cycling test, which means that failure occurred mainly at solder joints. Another benefit of eliminating underfill is that a new chip can be bonded on a reworked bond site since the chip mounting area can be easily cleaned. Therefore, the reworkability is largely improved.

To reveal the failure at the solder joints, as shown in Fig. 12, the failed samples were mounted with epoxy and cross-sectional polishing was performed in two directions. It can be seen that failure is mainly caused by cracking near the boundary between a solder joint and a Cu pad on the PWB. An important reason of such a failure is the excessive growth of Sn-Cu IMC close to the PWB Cu pads. As mentioned above, an obvious layer of IMC is observed in the as-bonded solder joint [Fig. 10(a)]. Since there was no effective barrier over the Cu pads on our present FR-4 board, IMC can grow at elevated temperature and result in a brittle joint close to the solder-Cu boundary, which has been reported for the Sn-rich solder alloys (60Sn40Pb, eutectic 63Sn37Pb, etc.) in flip-chips [15]. A solution to this issue is to use proper board finishes such as Ni that can act as a diffusion barrier as suggested in [15] and [16].

Other issue includes the poor solder mask opening design on the PWB. From Fig. 10(a), we can observe sharp solder mask edges at the solder-Cu pad, which may introduce stress concentration on the solder joints. The failure is observed mostly at the solder joints close to the edge of the chip, which is understandable because a larger global mismatch can be expected. The local mismatch has little effect due to the compliance of

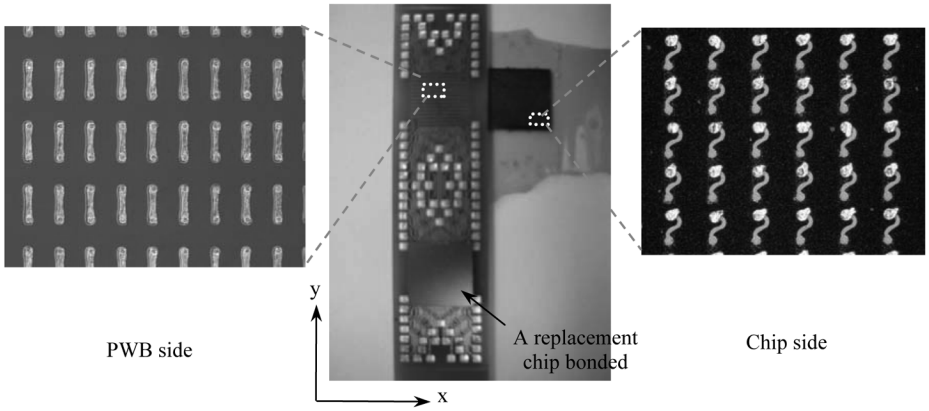
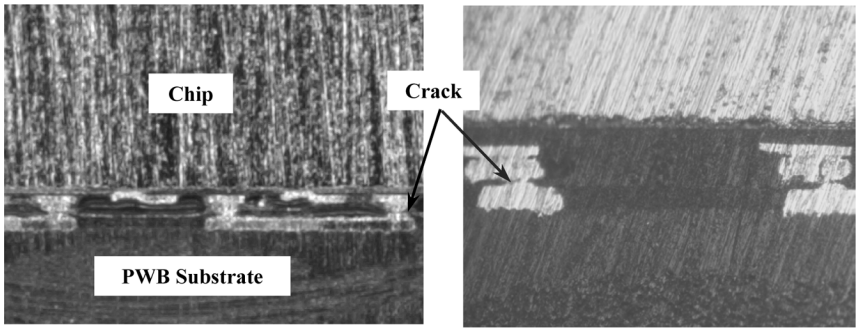


Fig. 11. Illustration of failure observation by removal of a failed chip at high temperature.



(a) polished in longitude (x) direction (b) polished in transverse (y) direction

Fig. 12. Cross-sectional failure observation by polishing of the failed sample in two directions.

the MEMS interconnects. Because of these reasons, we conclude that the main failure mechanism of this specific experiment is the early failure of the nonideal solder joints. Once reliable solder joining is achieved, the reliability potential of the MEMS leads can be fully demonstrated in the future work. Nevertheless, without use of underfill, the SoL MEMS interconnects have survived more than 500 thermal cycles, which indicates a promising improvement over a regular C4 solder interconnection. It is well known that a C4 solder joint usually cannot survive more than ~ 100 cycles on FR-4 substrates without underfill due to the CTE mismatch [17]. Moreover, reliability of the SoL MEMS interconnects can be further improved by optimization of chip-package codesign. For example, for a given I/O pitch, the lead geometry can be redesigned to increase the mechanical compliance. The lead orientation may also be rearranged so that the displacement direction of the "slippery" leads is close to the contour away from the neutral point position.

VI. Conclusion

For the first time, technology feasibility of a low-cost MEMS-type SoL I/O interconnects has been demonstrated through a full procedure of fabrication, assembly and reliability assessment. Process integration issues with a standard BEOL process have been addressed with three mask steps in addition to the conventional C4 solder bumping. FEA simulation illustrated that a compliant lead induces much smaller shear force on a chip pad compared to that from a C4 solder joint, which means a smaller impact on the chips with mechanically fragile low-K dielectrics. The need for underfill can be eliminated by the SoL MEMS interconnects since the compliant leads can compensate for the CTE mismatch.

Using a flip-chip bonder, the test chips with the SoL interconnects were assembled on the low-cost organic PWB test vehicles. Without underfill, the SoL MEMS interconnects survived more than 500 thermal cycles, which indicates a promising improvement over a regular C4 solder joint. Failure analysis revealed that the MEMS leads did not fracture during the tests, while the nonreliable joining at the nonoptimized PWB substrate is the main failure cause. The full reliability potential of the MEMS leads can only be demonstrated after a more reliable joining is achieved. Therefore, future work will include material optimization (solder, board metallurgy, etc.) and design optimization (solder joint dimension, lead geometry, and solder mask opening, etc.).

Acknowledgment

The authors are grateful to Promerus, LLC and Dr. P. Joseph in the Microelectronics Research Center at the Georgia Institute of Technology for supplying the polymer materials (Avatrel 2000P and Unity 200). Thanks are given to Dr. P. S. Andry in IBM T. J. Watson Research Center for his help with thermal cycling test. The authors are also thankful to K. Karker in School of Mechanical Engineering at Georgia Institute of Technology for his help with FEA modeling and part of the testing.

REFERENCES

[1] *Int. Technol. Roadmap of Semiconductor (ITRS)*, 2003 edition.

[2] L. L. Mercado, S.-M. Kuo, C. Goldberg, and T. Y. Lee, "Analysis of flip-chip packaging challenges on Copper/Low-k interconnects," *IEEE Trans. Device Mater. Reliab.*, vol. 3, pp. 111–118, 2003.

[3] G. Wang, C. Merrill, J. Zhao, S. K. Groothuis, and P. S. Ho, "Packaging effects on reliability of Cu/Low-k interconnects," *IEEE Trans. Device Mater. Reliab.*, vol. 3, pp. 119–128, 2003.

[4] L. L. Mercado, S.-M. Kuo, C. Goldberg, and D. Frear, "Impact of flip-chip packaging on Copper/Low-k structures," *IEEE Trans. Adv. Packag.*, vol. 26, pp. 433–439, 2003.

[5] J. Novitsky and D. Pedersen, "FormFactor introduces an integrated process for wafer level packaging, burn-in test, and module level assembly," in *Proc. Int. Symp. Adv. Packag. Mater.*, 1999, pp. 226–231.

[6] V. Solberg, D. Light, and J. Fjelstad, "Reliable and low cost wafer level packaging," in *Proc. IEEE/CPMT Int. Electron. Manufact. Technol. Symp.*, 2000, pp. 108–114.

[7] Q. Zhu, L. Ma, and S. K. Sitaraman, "Design optimization of one-turn helix: A novel compliant off-chip interconnect," *IEEE Trans. Adv. Packag.*, vol. 26, pp. 106–112, 2003.

[8] ——, "β-Helix: A lithography-based compliant off-chip interconnect," *IEEE Trans. Compon. Packag. Technol.*, vol. 26, pp. 582–590, 2003.

[9] M. S. Bakir, H. A. Reed, H. D. Thacker, C. S. Patel, P. A. Kohl, K. P. Martin, and J. D. Meindl, "Sea of leads (SoL) ultrahigh density wafer-level chip Input/Output interconnections for gigascale integration (GSI)," *IEEE Trans. Electron Devices*, vol. 50, pp. 2039–2048, 2003.

[10] M. S. Bakir, B. Dang, R. Emery, G. Vandentop, P. A. Kohl, and J. D. Meindl, "Sea of leads compliant I/O interconnect Process integration for the ultimate enabling of chips with low-k interlayer dielectrics," *IEEE Adv. Packaging*, vol. 28, no. 3, pp. 486–493, 2005.

[11] B. Dang, C. S. Patel, H. D. Thacker, M. S. Bakir, K. P. Martin, and J. D. Meindl, "Optimal implementation of sea of leads (SoL) compliant interconnect technology," in *Proc. IEEE Int. Interconnect Technol. Conf. (IITC)*, 2004, pp. 99–101.

[12] K. Hjort, J.-A. Schweitz, and B. Hok, "Bulk and surface micromachining of GaAs structures," in *Proc. IEEE Micro Electro Mechan. Syst.*, 1990, pp. 73–76.

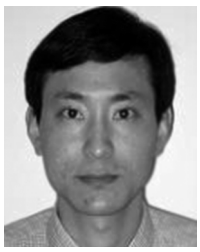
[13] T. Cristenson and H. Guckel, "Micro mechanics: An emerging technology," in *Proc. IEEE Int. SOI Conf.*, 1994, pp. 3–5.

[14] J. Jayachandran, H. Reed, H. Zhen, L. Rhodes, C. Henderson, S. Allen, and P. Kohl, "Air-channel fabrication for microelectromechanical system via sacrifical photosensitive polycarbonates," *J. Microelectromech. Syst.*, vol. 12, no. 2, pp. 147–159, 2003.

[15] S. Y. Jang and K. W. Paik, "Comparison of electroplated eutectic Bi/Sn and Pb/Sn solder bumps on various UBM systems," *IEEE Trans. Electron. Packag. Manuf.*, vol. 24, no. 4, pp. 269–274, 2001.

[16] K. C. Chan, Z. W. Zhong, and K. W. Ong, "Investigation of Cr/Cu/Cu/Ni under bump metallization for lead-free applications," in *Proc. 4th Electron. Packag. Technol. Conf.*, 2002, pp. 270–275.

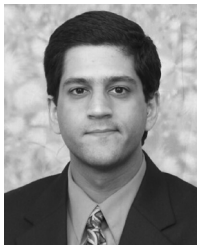
[17] L. Chen, Q. Zhang, G. Wang, X. Xie, and Z. Cheng, "The effects of underfill and its material models on thermomechanical behaviors of a flip chip package," *IEEE Trans. Adv. Packag.*, vol. 24, pp. 17–24, 2001.



Bing Dang (S'01) received the B.S. and M.S. degrees in metallurgical physical chemistry from the University of Science and Technology, Beijing, China, in 1995 and 1998, respectively. He also received the M.S. degree in materials engineering and another M.S. degree in electrical and computer engineering from Auburn University, Auburn, AL, in 2000 and 2002, respectively.

He is currently pursuing the Ph.D. degree in electrical and computer engineering at the Georgia Institute of Technology, Atlanta. His primary research interests include the integrated interconnection and packaging technologies for gigascale integrated circuits, thermal management, and MEMS. He has authored and/or coauthored 20 publications in journals and peer-reviewed international conference proceedings.

Mr. Dang received the Auburn University Graduate Research Fellowship (1998–2001) and was recognized as an Outstanding Graduate Student in College of Engineering at Auburn University (1999–2000).



Muhannad S. Bakir (S'99–M'04) received the B.E.E. degree (*summa cum laude*) from Auburn University, Auburn, AL, in 1999. He received the M.S.E.E. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology, Atlanta (Georgia Tech), in 2000 and 2003, respectively.

He is currently a Research Engineer II with the Microelectronics Research Center and an Adjunct Professor with the School of Electrical and Computer Engineering, Georgia Tech. His primary area of interest is developing long-term integrated electrical, optical, and fluidic I/O interconnection, and packaging technologies for gigascale integration. He has published more than 30 refereed and invited publications that appear in conference proceedings and journals.

Dr. Bakir is a recipient of the Georgia Tech President's Fellowship (1999 to 2003) and the Intel Ph.D Fellowship (2002 to 2003). The awards he received while at Auburn University include the IEEE's Most Outstanding Graduating Senior from the Electrical and Computer Engineering Department, in spring 1999; and the International Engineering Consortium's William L. Everitt Student Award of Excellence in 1999. He was also on the Engineering Dean's Honor List for 10 quarters. He has been awarded a MARCO Inventor Recognition Award (2002) and is a recipient of the Best Conference Paper Award from the 2002 Electronic Components and Technology Conference (ECTC). He is a conference committee member for the IEEE LEOS Annual Meeting.

Chirag S. Patel received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Georgia Institute of Technology, Atlanta, in 1995, 1996, and 2001, respectively.

In 2001, he joined the IBM Research Division, Thomas J. Watson Research Center, Yorktown Heights, NY, where he is a Research Staff Member in the Science and Technology Department working on advanced and exploratory packaging technologies. He is an author or coauthor of more than 35 technical papers.

Hiren D. Thacker (M'00) received the B.S. and M.S. degrees in electrical engineering from the Georgia Institute of Technology, Atlanta (Georgia Tech), in 2000 and 2002, respectively.

He is currently a Ph.D. degree candidate with the School of Electrical and Computer Engineering at Georgia Tech. His research interests include microsystem integration and packaging; optical interconnects; and the design and processing of novel micro- and nanoscale devices for varied applications.

James D. Meindl (M'56–SM'66–F'68–LF'97) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Carnegie Institute of Technology, Carnegie-Mellon University, Pittsburgh, PA.

He is the Director of the Joseph M. Pettit Microelectronics Research Center and the Joseph M. Pettit Chair Professor of Microelectronics at the Georgia Institute of Technology, Atlanta. He is also Director of the Interconnect Focus Center, a multiuniversity research effort managed jointly by the Microelectronics Advanced Research Corporation and the Defense Advanced Research Projects Agency for the Department of Defense. His current research interests focus on physical limits on gigascale integration and nanotechnology.

Prof. Meindl is a Life Fellow of the American Association for the Advancement of Science and a Member of the American Academy of Arts and Sciences and the National Academy of Engineering. In September 2004, he was presented with the 2004 SRC Aristotle Award, recognizing outstanding teaching in its broadest sense. He was awarded first place on the IEEE International Solid State Circuits Conference 50-Year Anniversary Author Honor Roll, 2003. He received the Georgia Institute of Technology 2001 Class of 1934 Distinguished Professor Award, the IEEE Third Millenium Medal in 2000, the 1999 SIA University Research Award, and the 1997 Hamerschlag Distinguished Alumnus Award from Carnegie-Mellon University.